Figure 1. 8-bit ADC using the ADC0808, 8-bit 8 channel ADC. EOC can be connected to the processor interrupt input or to a polled input port.

Figure 2

\[ I_{R14} = 5mA \quad V_{REF} = 5\text{ volts} \]

Figure 3. 8-bit DAC

Figure 4. equation governing the DAC output
1. Define: (a) resolution of DAC and ADC (b) settling time (c) ½ LSB error (3 pts)
2. Determine the resolution of the ADC in Figure 1 in terms of the lowest resolvable input voltage. (2 pts)
3. Determine the input voltage that is represented by the binary number 100011012 at the ADC output. (5 pts)
4. Interface the ADC in Figure 1 to an 8088 microprocessor system. Design the ADC address decoder to respond to address 0300\text{H}. Draw the detailed block diagram for (a) polled IO design and (b) interrupt driven IO. Assume no interrupt controller used. (10 pts)
5. Draw the flowchart to drive the ADC in (4) assuming that the timing diagram for the ADC in figure 1 is given in figure 5. Assume further that that the analog input is connected in input 5. (10 pts)
6. Interface the DAC in figure 3 to the 8086 system in (4). Use port address 400\text{H}. Draw the detailed block diagram. (5 pts)
7. Draw the flowchart of the software driver that will generate a ramp at the output of the DAC. (5 pts)
8. Using the parameters given in figure 4 for the DAC in figure 3, determine the voltage step assuming \( \text{R}_\text{L} = 5\text{K ohms} \). (5 pts).
9. For an output voltage of 2.75 volts to be generated at the output of the DAC, what is the binary value that must be input to the DAC. (5 pts)

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**Figure 5. ADC Timing Diagram**

![Timing Diagram](image-url)